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Claims 8 and 10 have been amended to correct what will be readily recognized as typographical errors.

Non-elected claims 11-16 have been canceled without prejudice or disclaimer. Applicants reserve the right to file a divisional application directed to the subject matter of the non-elected claims prior to the termination of proceedings in this application or any application claiming priority therefrom.

Claims 1-3 and 6 were rejected under 35 U.S.C. Section 102(b) as allegedly being anticipated by Akram (U.S. Patent No. 5,736,446). While not acquiescing in this rejection, claim 1 has been amended. As such, the applied art is discussed below with reference to the amended claim.

Claim 1 calls for a semiconductor device in which a main conductor layer is electrically connected to an electrode pad; an insulating layer has an opening section on the main conductor layer; and a protrudent electrode is electrically connected to the main conductor layer via the opening section. A metal layer is provided only on a bottom surface of the opening section on the main conductor layer so that the metal layer is provided between the main conductor layer and the protrudent electrode. Akram at least fails to disclose the claimed metal layer. In particular, Akram discloses a method for forming conductive bumps in which a metal layer is provided on the bottom surface and on sidewalls of an opening section. See, *e.g.*, Figures 3c and 3d. In Akram, because a bump is connected to the bottom surface and sidewalls of an opening section in a passivation layer, an alloy layer is formed on the bottom surface and the sidewalls. The alloy layer exists in the vicinity of the passivation layer and the conductive trace. However, because of the difference in linear expansion coefficient between the passivation layer and the conductive trace, the alloy layer becomes stressed when temperature changes. Such stress causes

cracks in the alloy layer, and cracks develop even inside the bump, thereby resulting in the possibility of connection failure. In contrast, the claimed semiconductor device does not have such a problem because the metal layer is formed only on the bottom surface of the opening section on the main conductor layer, and the above-described cracks do not occur.

In addition, Akram requires a step of removing an unnecessary metal layer by CMP after the metal layer is formed in the opening section of the passivation layer. See, *e.g.*, Figures 3a and 3b. The claimed semiconductor device offers the possibility, if desired, of being formed using a simpler manufacturing process because the metal layer can be formed only on the bottom surface of the opening section.

For at least these reasons, Applicants submit that Akram cannot anticipate the subject matter of claims 1-3 and 6.

Claims 1, 4 and 5 were rejected under 35 U.S.C. Section 103(a) as allegedly being obvious over Akram. In particular, it is alleged in the office action that the use of certain materials and a layer of a certain thickness would have been obvious in view of Akram. While not acquiescing in these conclusory contentions, there is not teaching or suggestion in Akram of providing a metal layer only on a bottom surface of the opening section on the main conductor layer as discussed above. For at least these reasons, Akram cannot render obvious claim 1 or claims 4 and 5 which depend therefrom.

Claims 1 and 7-9 were rejected under 35 U.S.C. Section 103(a) as allegedly being obvious over Akram in view of Okada *et al.* (U.S. Patent No. 6,111,317). Okada *et al.* however does not remedy the above-identified deficiencies of Akram with respect to claim 1. As such, even assuming (without admitting) the characterizations of Okada *et al.* in the office action are

correct and that the combination of Akram and Okada *et al.* would have been proper, the subject matter of claim 1 and its dependent claims 7-9 would not result.

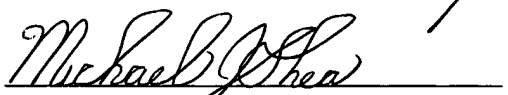
Claims 1 and 10 were rejected under 35 U.S.C. Section 103(a) as allegedly being obvious over Akram in view of Stamper *et al.* (U.S. Patent No. 6,362,531). Stamper *et al.* however does not remedy the above-identified deficiencies of Akram with respect to claim 1. As such, even assuming (without admitting) the characterizations of Stamper *et al.* in the office action are correct and that the combination of Akram and Stamper *et al.* would have been proper, the subject matter of claim 1 and its dependent claim 10 would not result.

New claims 17-28 have been added for the Examiner's consideration. The subject matter of these new claims is fully supported by the original disclosure and no new matter is added. These claims are believed to be allowable for reasons similar to those advanced above with respect to claims 1-10.

Applicants submit that the pending claims are in condition for allowance, and action to that end is earnestly solicited.

If any issues remain to be resolved, the Examiner is urged to contact the attorney for Applicants at the telephone number listed below.

Respectfully submitted,
NIXON & VANDERHYE P.C.



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Version marked to show changes made

IN THE SPECIFICATION

The paragraph beginning on page 3, line 15 has been amended as follows:

Talking about its manufacturing method, firstly the first protective insulating film 103 is formed on the semiconductor substrate 101 provide with the electrode pad 102. The first opening section 103a is formed on the first protective insulating film 103 so as to expose the electrode pad 102. The metal layer 104 is formed in the first opening section 103a and on the first protective insulating film 103, by sputtering [spattering] or vapor deposition. Subsequently, a resist is applied on the metal layer 104. An opening section is made in the resist so that exposure and development of the resist prepares an area in which the outgoing line 109 is formed.

The paragraph beginning on page 13, line 21 has been amended as follows:

The following describes a first embodiment of the present invention, referring to Figure 1 through [to] Figures 3(a) to 3(c).

The paragraph beginning on page 19, line 12 has been amended as follows:

Furthermore, regarding the semiconductor device as a whole, formed on the semiconductor substrate 1 is a wire pattern that is to be connected to the semiconductor element. On the wire pattern, a plurality of the electrode pads 2 are formed at intervals. The electrode

pads [pats] 2 are electrically connected to the wire pattern. Further, the first insulating layer 3 is formed on the wire pattern. Moreover, a plurality of the wires 6 are formed on the first insulating layer 3. The wires 6 have an end that is connected to the electrode pad 2 via the first opening section 3c. Moreover, the wires 6 detour so that they do not touch each other, and are connected to the external connection terminal 9.

The paragraph beginning on page 20, line 24 has been amended as follows:

Next, the first metal layer 4 is formed over the entire surface of the semiconductor substrate 1 by sputtering [spattering], in sequence that Ti-W is followed by Cu (Figure 2(a)). Then, in a photosensitive resist 11, a resist opening section 11a is created, by a photolithography method, on the region where the electrode pads 2 and wires 6 are formed. Subsequently, the second metal layer 5 is formed in the resist opening section 11a by electroplating of Cu (Figure 2(b)).

The paragraph beginning on page 27, line 14 has been amended as follows:

After the first insulating layer 3 is formed, the first metal layer 4 is formed all over the semiconductor substrate 1 by sputtering [spattering], where Ti-W is applied first, then Cu (Figure 5(a)). By employing the photolithography method that uses the photosensitive resist 17, a resist opening section 17a is created on the region where the electrode 2 and the wire 15 are formed. Subsequently, the second metal layer 5 is formed by performing electroplating of Cu in the resist opening section 17a. Further, on the second metal layer 5, electroplating of Ni is carried out for forming the fourth metal layer 14 (Figure 5(b)). Here, the electroplating of Ni is possible

because the first insulating layer 3 is formed on the entire surface of the semiconductor substrate 1.

The paragraph beginning on page 29, line 1 has been amended as follows:

With the above manufacturing method, the third metal layer 16 can be formed only in the second opening section 8a, as in the first embodiment. This causes no gap formation between the second insulating layer 8 and the wire 15, even when the third metal layer 16, which includes Au having the good wetting properties with respect to the Su-Pb solder structuring the external connection terminal 9, is diffused into the external connection terminal 9, because the diffusion of the third metal layer 16 takes place only in the second opening section 8a. This prevents the water condensation in the gap formed between the second insulating layer 8 and wire 15, and avoids the connection failure caused by the water condensation. Therefore, the semiconductor device of the high connection reliability can be attained. Furthermore, the thickness of the third metal layer 16 can be thinner, so that stress load on the side wall of the second opening section 8a can be reduced at the time of the electroless plating of Au in the second opening section 8a, and exfoliation and cracking [crack] of the second insulating layer 8 can be prevented.

The paragraph beginning on page 30, line 9 has been amended as follows:

Here, described below is an example of a manufacturing process of the present embodiment, where the top and side surfaces of the second metal layer 5 are [is] coated with the fourth metal layer 14, with reference to Figures 7(a) through 7(c). Note that, the manufacturing process has a step identical with that of the manufacturing process discussed earlier, up to Figure

5(a) where the first metal layer 4 is formed. Thus, the explanation of [on] the step is not repeated, and the rest of the steps are discussed, here.

The paragraph beginning on page 33, line 14 has been amended as follows:

Also with the manufacturing method, as the semiconductor device discussed previously, by covering the top and side surfaces of the second metal layer 5 with the fourth metal layer 14 made of Ni, it is possible to prevent the water condensation in the gap formed between the second insulating layer 8 and the wire 15, which may cause [the] connection failure, and exfoliation and cracks of the second insulating layer 8. Therefore, the semiconductor device having [the] high connection reliability can be attained.

The paragraph beginning on page 34, line 3 has been amended as follows:

With the above arrangement, the protrudent [protrude] electrode is made of Sn or a [the] metal having Sn as its main component, while the metal layer is made of Au or a [the] metal having Au as its main component. This gives the protrudent electrode good wetting properties, thereby adhesion of the protrudent electrode is better, compared to a case where the metal layer, which is in contact with the protrudent electrode, is made of a metal in the platinum group.

The paragraph beginning on page 36, line 8 has been amended as follows:

A [An] semiconductor device is preferably provided with a barrier metal layer made of Ni or a metal having Ni as its main component, on an entire top surface of the main conductor layer.

The paragraph beginning on page 37, line 10 has been amended as follows:

A [An] semiconductor device is preferably further provided with a foundation metal layer made of Ti, Ti-W, Cr, or a metal having any of those elements as its main component, under the main conductor layer.

IN THE CLAIMS

Claims 1, 8 and 10 have been amended as follows:

1. (Amended) A semiconductor device, comprising:

a main conductor layer having an end that is electrically connected to an electrode pad;

an insulating layer having an opening section on said main conductor layer; and

a protrudent electrode electrically connected to said main conductor layer via said opening section,

said semiconductor device[,] further comprising:

a metal layer provided only on a bottom surface of the opening section on the main conductor layer [in the opening section] so that said metal layer is provided between said main conductor layer and said protrudent electrode.

8. (Amended) The [An] semiconductor device as set forth in Claim 1, further comprising:

a barrier metal layer made of Ni or a metal having Ni as its main component, on an entire top surface of said main conductor layer.

10. (Amended) The [An] semiconductor device as set forth in Claim 1, further comprising:

a foundation metal layer made of Ti, Ti-W, Cr, or a metal having any of those elements as its main component, under said main conductor layer.